

LATERAL FET STRUCTURE WITH IMPROVED BLOCKING VOLTAGE AND ON  
RESISTANCE PERFORMANCE AND METHOD

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Abstract of the Disclosure

In one embodiment, a lateral FET structure (30) is  
formed in a body of semiconductor material (32). The  
10 structure (30) includes a plurality non-interdigitated drain  
regions (39) that are coupled together with a conductive  
layer (57), and a plurality of source regions (34) that are  
coupled together with a different conductive layer (51).  
One or more interlayer dielectrics (53,54) separate the two  
15 conductive layers (51,57). The individual source regions  
(34) are absent small radius fingertip regions.